# PCB Layout and Design Guide for CH7117 HDMI to SDTV/HDTV/LVDS/BT656 Converter with Flexible Scaler

## 1.0 INTRODUCTION

The CH7117 is an innovative semiconductor device that consists of HDMI receiver, three separate 9-bit video Digital-to-Analog Converters (DACs), SDTV encoder, HDTV encoder, YCbCr 4:2:2 encoder, VGA and audio encoder, which can convert HDMI signals into CVBS/S-Video/YPbPr/VGA/LVDS/BT656 outputs with IIS or SPDIF audio output. The CH7117 satisfies manufactures' products display requirements and reduce their costs of development and time-to-market.

This application note focuses only on the basic PCB layout and design guidelines for CH7117. Guidelines in component placement, power supply decoupling, grounding, input /output signal interface are discussed in this document.

The discussion and figures that follow reflect and describe connections based on the 88-pin QFN package of the CH7117. Please refer to the CH7117 datasheet for the details of the pin assignments.

## 2.0 COMPONENT PLACEMENT AND DESIGN CONSIDERATIONS

Components associated with the CH7117 should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

### 2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1μF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These 0.1μF capacitors should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7117 ground pins, in addition to ground vias.

#### 2.1.1 Ground Pins

The analog and digital grounds of the CH7117 should be connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7117 ground pins should be connected to its respective decoupling capacitor ground lead directly, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. Refer to **Table 1** for the Ground pins assignment.

#### 2.1.2 Power Supply Pins

Refer to **Table 1** for the Power supply pins assignment. Refer to **Figure 1** for Power Supply Decoupling.

**Table 1: Power Supply Pins Assignment of the CH7117**

| Pin Assignment | # of Pins | Type | Symbol | Description |
|---|---|---|---|---|
| 5,15,20,37,51, 73,86 | 7 | Power | AVCC_33 | Analog 3.3V Power Supply (3.3V) |

| | | | | |
|---|---|---|---|---|
| 55, 59 | 2 | Power | AVCC_DAC | DAC Power supply (3.3V) |
| 18,38,53 | 3 | Power | DVDD | Digital 1.2V Power supply (1.2V) |
| 7,25,42,64 | 4 | Power | AVCC_12 | Analog 1.2V Power supply (1.2V) |
| 39 | 1 | Power | VDD_DDR | Digital Power supply (1.8V) |
| 76 | 1 | Power | VDDQ_DDR | Digital Power supply (1.8V) |
| 6,12,26,41,50, 57,61,65,74 | 9 | Ground | AVSS | Analog Ground |
| 19,40,52 | 1 | Ground | DGND | Digital Ground |
| Thermal Exposed Pad | | Ground | | Connect to ground plane through thermal via |

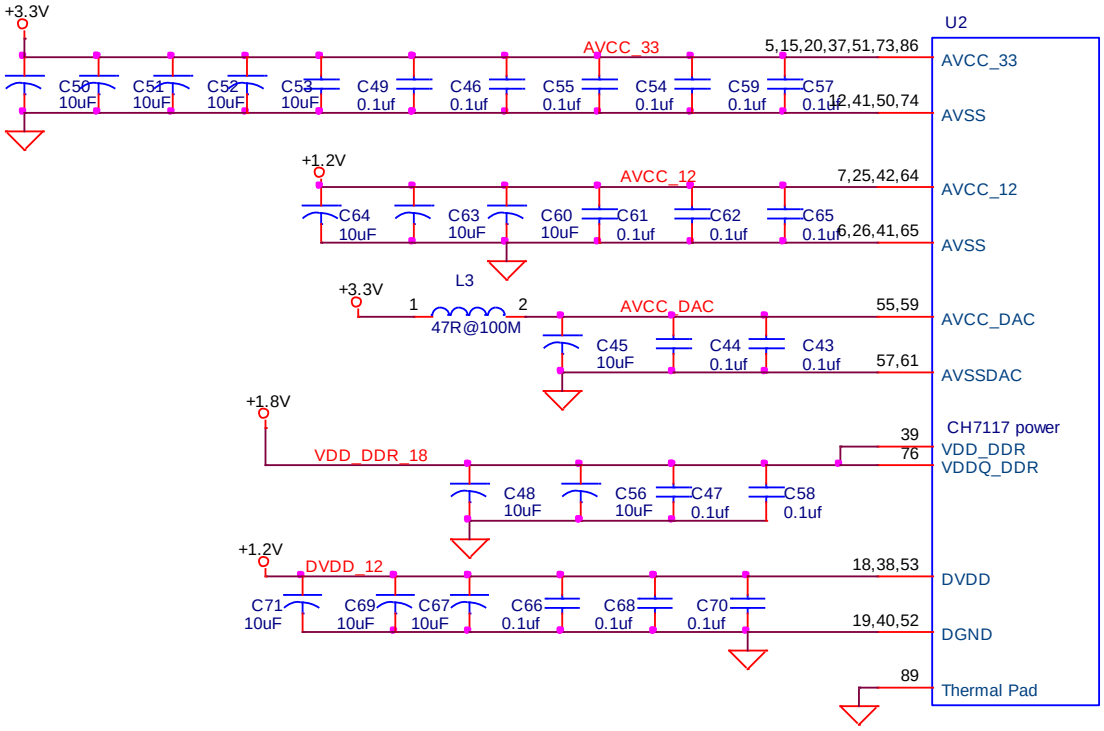


**Figure 1: Power Supply Decoupling and Distribution**

**Note:** All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05 Ω at DC; 23 Ω at 25MHz & 47 Ω at 100MHz. Please refer to Fair Rite part #2743019447 for details or an equivalent part can be used for the diagram.

## 2.2 Power On and Reset

RSTB pin is the chip reset pin of CH7117. CH7117 will be reset when this pin is low. A power reset switch can be placed on the RSTB pin on the PCB as hardware reset for CH7117 as shown in **Figure 5**. When the pin is high, the reset function can also be controlled through the serial port.

There are two reset methods. One is RC reset. The power supply should be valid and stable for at least 9ms before RSTB becomes invalid as shown in **Figure 2**. A 1 MΩ and 0.1uF RC reset circuit is recommended.

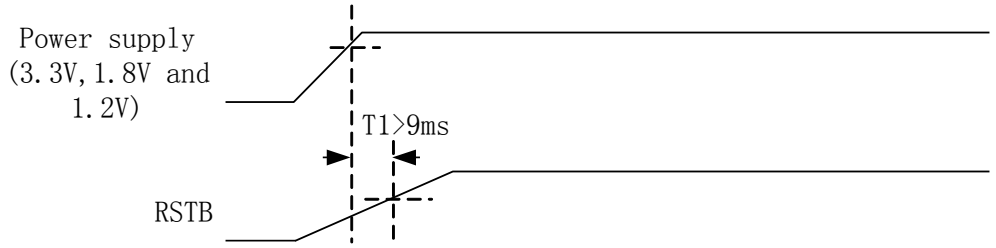


**Figure 2: Power on and reset timing of RC**

Another method is using an external reset signal. In this case, the power supply should be valid and stable for at least 9ms before the reset signal is valid. The pulse width of valid reset signal should be at least 100us. The timing is shown in **Figure 3.**

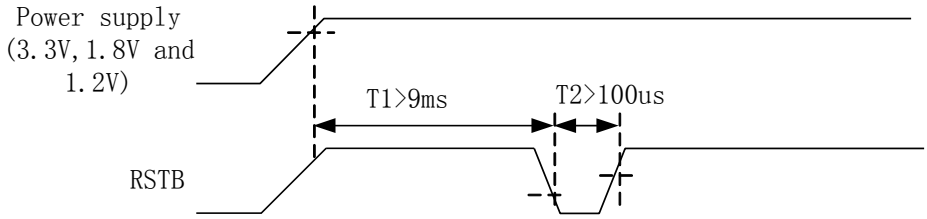


**Figure 3: Power on and reset timing of external reset**

Note: 1. The power supply will be valid when it rises to 90% of standard level.
2. The rising time (10%~90%) of power supply shall not exceed 2.5ms.
3. The rising threshold of RSTB is 2.4V.
4. The falling threshold of RSTB is 0.4V.

**Reset and CH7117 State**
After the reset operation of CH7117 is finished, CH7117 need maxim 308.65ms time to load firmware in flash and EEPROM. During firmware loading, CH7117 should be not accessed by external interface. The timing is shown in **Figure 4.**

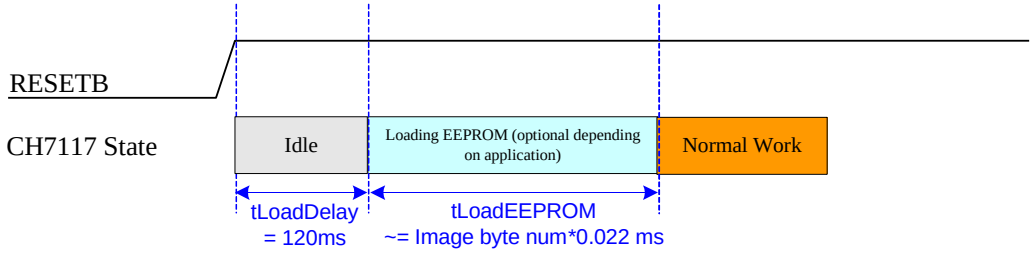


**Figure 4: Reset and CH7117 State**

## 2.3 General Control Pins

**• ISET and RESERVED**

ISET pin sets the basic current. A 1 KΩ, 1% tolerance resistor should be connected between this pin and Ground plane with short and wide traces and a ground via as shown in **Figure 5.**If there is no advice from Chrontel, do not adjust the value of resistor. The noise of Iset should be lower than -83dBm. A 100pf (not above 360pf) capacitor in parallel with Iset resistor can be used to suppress noise.

The RESERVED pins (Pin67) should be pulled low through a 10 KΩ resistor.

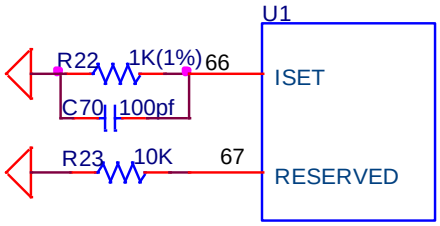


**Figure 5: ISET pin and RESERVED Pin67**

**• XI and XO**

CH7117 needs a 27M crystal to generate a reference clock.

The crystal load capacitance, $C_L$, is usually specified in the crystal spec from the vendor. As an example to show the load capacitors, **Figure 6** gives a reference design for crystal circuit design.

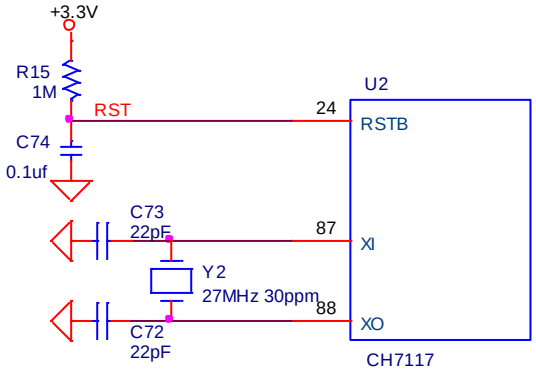


**Figure 6: General Control Pins**

**• Reference Crystal Oscillator**

CH7117 includes an oscillator circuit that allows a predefined-frequency crystal to be connected directly. Alternatively, an externally generated clock source may be supplied to CH7117. If an external clock source is used, it should have CMOS level specifications. The clock should be connected to the XI pin, and the XO pin should be left open. The external source must exhibit ±100 ppm or better frequency accuracy, and have low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

The crystal is specified to be predefined-frequency, ±30 ppm fundamental type and in parallel resonance (NOT series resonance). The crystal should also have a load capacitance equal to its specified value ($C_L$).

External load capacitors have their ground connection very close to CH7117 ($C_{ext}$).

To be able to tune, a variable capacitor may be connected from XI to ground.

Note that the XI and XO pins each has approximately 10 pF ($C_{int}$) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI and XO pins, the following calculation should be used:

$\mathbf{C}_{ext} = (2 \times C_L) - C_{int} - 2C_S$

Where
$C_{ext}$ = external load capacitance required on XI and XO pins.
$C_L$ = crystal load capacitance specified by crystal manufacturer.
$C_{int}$ = capacitance internal to CH7117 (approximately 10-15 pF on each of XI and XO pins).

$C_S$ = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

In general,
$C_{int}XI = C_{int}XO = C_{int}$
$C_{ext}XI = C_{ext}XO = C_{ext}$

such that $C_L = (C_{int} + C_{ext}) / 2 + C_S$ and $C_{ext} = 2 (C_L - C_S) - C_{int} = 2C_L - (2C_S + C_{int})$

Therefore $C_L$ must be specified greater than $C_{int}/2 + C_S$ in order to select $C_{ext}$ properly.

After $C_L$ (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is not operating in an excessive drive level specified by the crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

For detail considerations of crystal oscillator design, please refer to **AN-06**.

## 2.4 Serial Port Control for CH7117

**• SPC and SPD**

SPD and SPC function as a serial interface where SPD is bi-directional data and SPC is an input only serial clock. In the reference design, SPD and SPC pins are pulled up to 3.3V with 6.8 KΩ resistors as shown in **Figure 7**.

**• SPCM and SPDM**

SPDM and SPCM are used to interface with an external EEPROM. SPDM and SPCM pins should be pulled up to 3.3V with 6.8 KΩ resistors as shown in **Figure 7**.

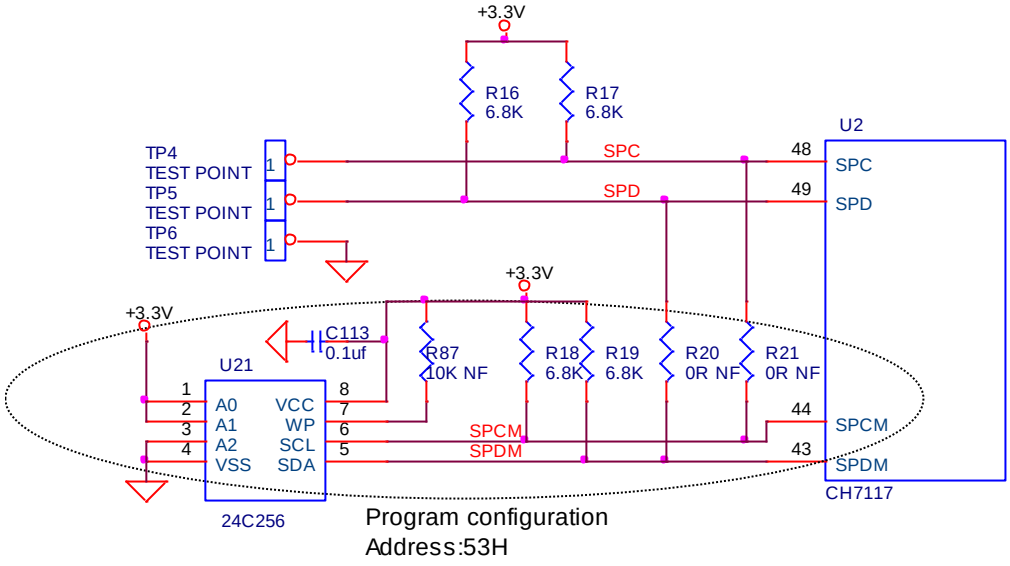


**Figure 7: Serial Port Interface of CH7117**

## 2.5 Audio Interface

CH7117 supports I2S or SPDIF audio output.

**• SPDIF Interface**

The pin 70 (I2STX_DATA/SPDIFTX) is a multi-function input pin. It can be configured to SPDIF audio output pin or IIS data output pin.

The SPDIF signal has two voltage levels, so there are two output ways for CH7117. If COMS or TTL level (3.3V~5V) of SPDIF signal is required, it can be connected to the CH7117 directly. If COAX level (0.5V~1V) of SPDIF signal is required, a resistor divider is needed as shown in **Figure 8**.

**• I2S Interface**

I2S audio output can be configured through programming CH7117 registers. An I2S bus design consists of four serial bus lines: a line with data channel [SD], a word select line [WS], a clock line [SCK], and an optional clock line [MCLK]. Data is transmitted two's complement, MSB first.

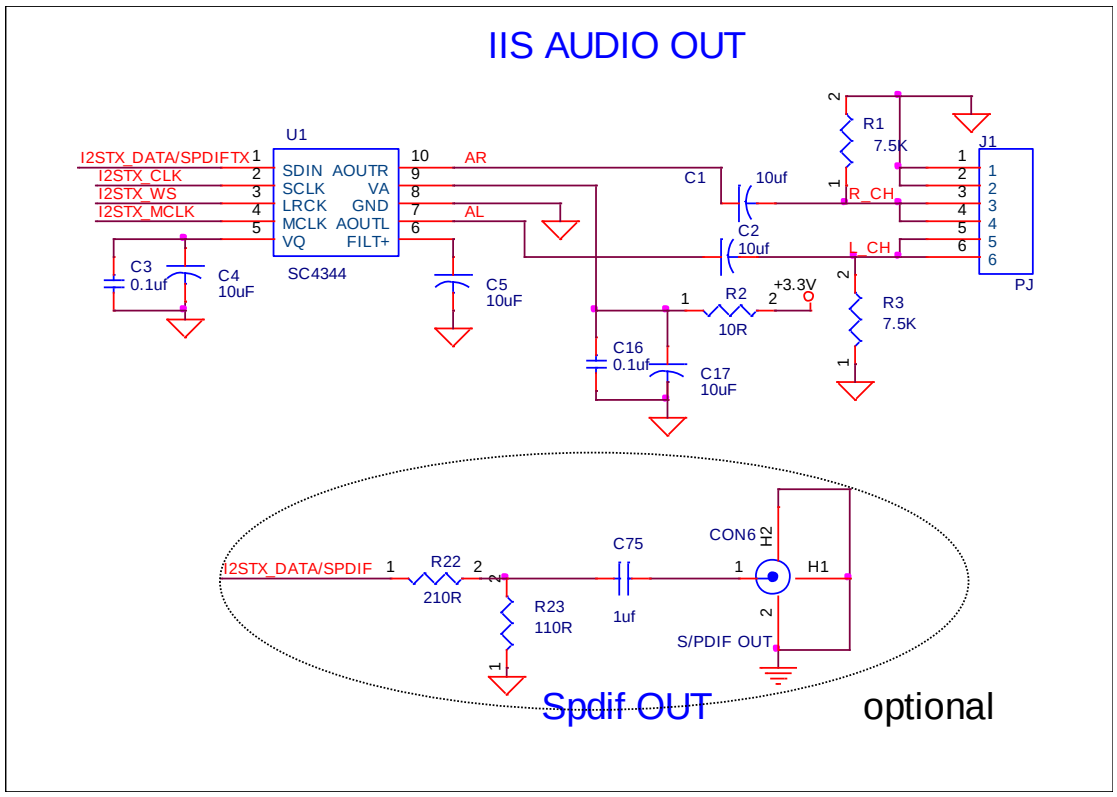


**Figure 8: CH7117 SPDIF and IIS Ouput Pins**

## 2.6 GPIO Pins

CH7117 has five GPIO pins. All GPIO pins can be configured as input or output.

As default, GPIO1 and GPIO4 are used as input pin to select output mode of CH7117, GPIO0, GPIO2 and GPIO3 are used to select CVBS output mode as shown in **Figure 9**.

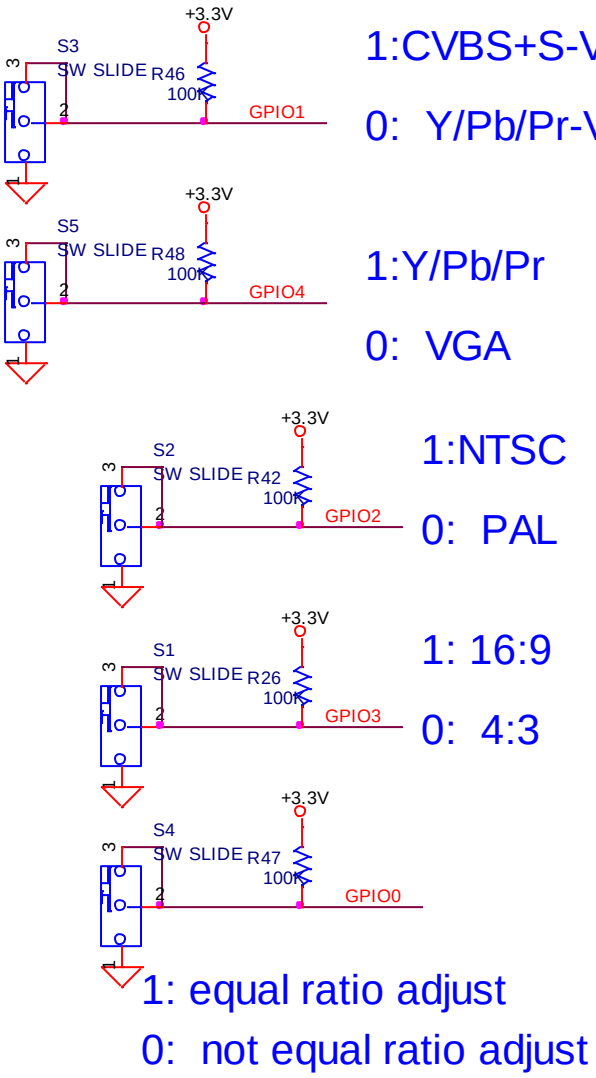


**Figure 9: CH7117 GPIO Pins**

## 2.7 LVDS Input and Output

CH7117 can support one lane LVDS output and input.

### 2.7.1 LVDS Input Interface

CH7117 can accept 18bit or 24bit SPWG/OpenLDI format data from LVDS transmitter.

CH7117 LVDS input channel differential pairs have optional internal termination resistors of 100Ω inside. It has the advantage of terminating as close as possible to the receiver (minimizing stubs) and also saving board space and reducing component count.

### 2.7.2 LVDS Onput Interface

LVDS output is shown in **Figure 10**.

CH7117 can be configured as 18bit or 24bit SPWG/OpenLDI format data. The LVDS TX pin order and polarity can be configured by register.

CH7117 LVDS Output channel differential pairs have optional internal termination resistors of 100Ω inside.

In order to facilitate LVDS loop test, the following pin pairs are swapped by firmware default configuration.

TXC/TXCB<-> TX3/TX3B

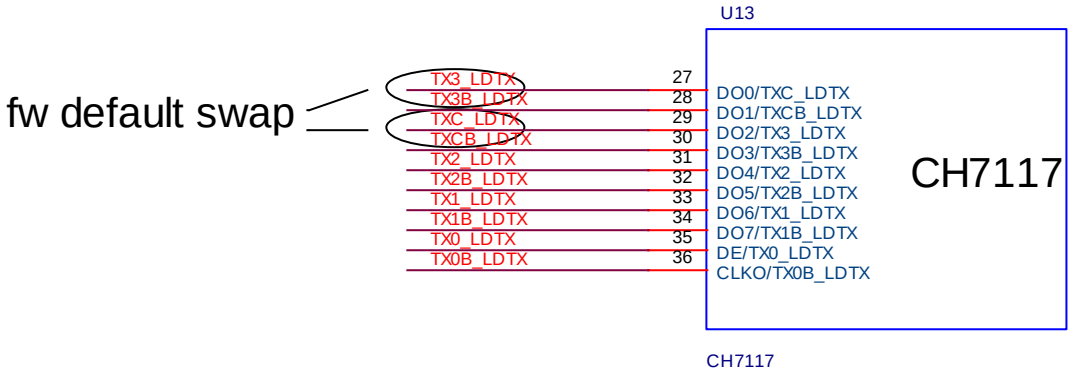


**Figure 10：CH7117 LVDS output Pins**

CH7117 has backlight control function. GPIO0, GPIO1, GPIO2 can be configured as ENABKL, ENPWR, PWM. LVDS backlight control circuit is shown in **Figure 11**.

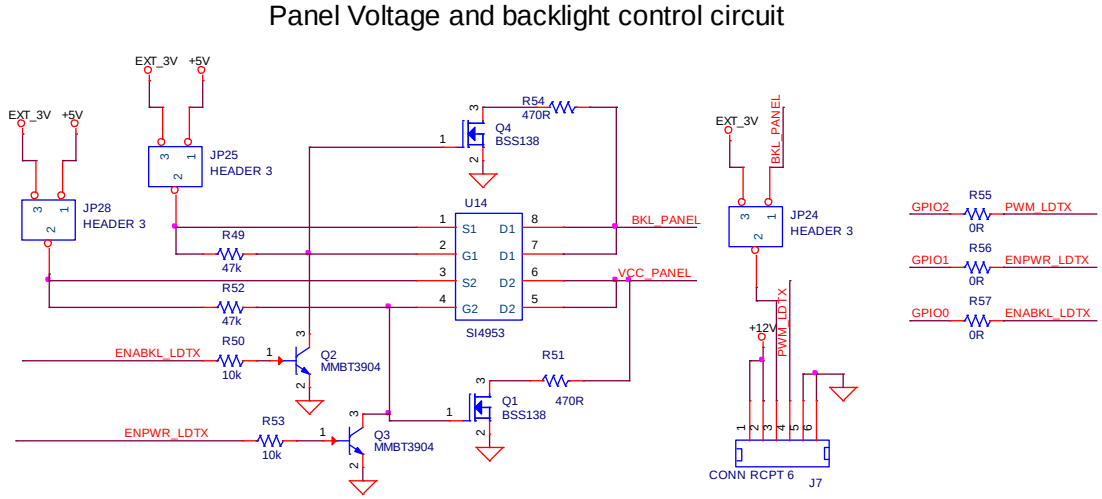


**Figure 11: LVDS Panel Voltage and Backlight Control Circuit**

### 2.7.3 LVDS Differential Trace Layout

Since LVDS signals are differential, they must be routed in differential pairs. The differential impedance of LVDS pairs should be 100Ω. It is recommended that 5 mils traces should be used in routing these signals. There should be 7 mils spacing between each intra pair.
The length for a pair of intra differential signals should be matched within 5 mils. The length for inter pairs should be matched within 100 mils.

Bend which is smaller than 45 degrees should be avoided.

The differential pairs should be placed above solid ground plane or power plane to minimize un-continued impedance.

Smallest size vias and connector pads are recommended to be used. It is recommended that 12 mils inner diameter and 18 mils outer diameter vias or smaller one should be used in routing these signals.

To maintain constant differential impedance along the length, it is important to keep the trace width and spacing

uniform along the length, as well as maintain good symmetry between the two lines.

## 2.8 BT656 Input and Output

CH7117 can support 8 bit YCbCr 4:2:2 (BT656) embedded sync input (**Figure 12**), and normal sync or embedded sync output format. (Refer to **Figure 13**)

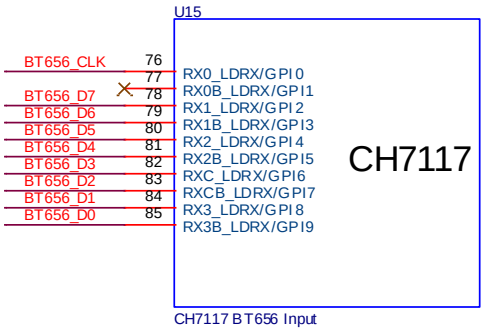


**Figure 12: CH7117 BT656 input**

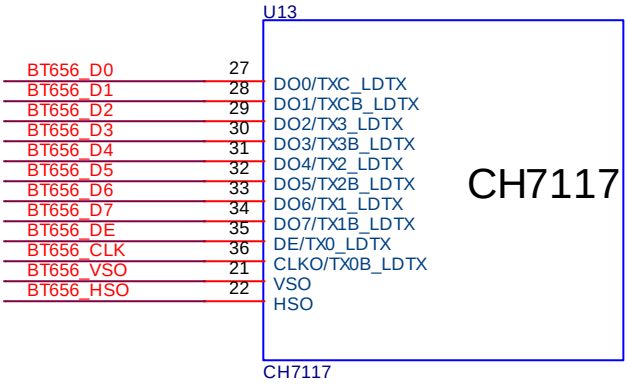


**Figure 13: CH7117 BT656 output**

## 2.9 HDMI Input

The four differential signals, RXCB_HMRX and RXC_HMRX, RX0B_HMRX and RX0_HMRX, RX0B_HMRX and RX0_HMRX, RX0B_HMRX and RX0_HMRX, are high frequency differential signals that need to be routed with special precautions. Since those signals are differential, they must be routed in differential pairs.

### 2.9.1 Differential Pair Impedance

To match the external cable impedance and maintain the maximal energy efficiency it is important to meet the impedance target of 100 Ω ± 10% for the differential data/clock traces. The restriction of this impedance target is to prevent any loss of signal strengths resulting from a reflection of unwanted signals. The impedance can be acquired by proper design of trace length, trace width, signal layer thickness, board dielectric, etc. The HDMI differential pairs should be routed on the top layer directly to the HDMI connector pads if possible.

### 2.9.2 Trace Routing Length

To prevent from capacitive and impedance loading, trace lengths should be kept as minimal as possible. Vias and bends should always be minimized; inductive effects may be introduced, causing spikes in the signals. Trace routing lengths from CH7117 to the HDMI/DVI connector are limited to a maximum of 2 inches. The CH7117 should be as close to the HDMI/DVI connector as possible.

### 2.9.3 Length Matching for Differential Pairs

The HDMI/DVI specifies the intra-pair skew and the inter-pair skew as in **Table 2**. The intra-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between the true and complement signals. The inter-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between any two single-ended data signals that do not constitute a differential pair.

**Table 2: Maximum Skews for the HDMI/DVI Transmitter**

| Skew Type | Maximum at Transmitter |
|---|---|
| Intra-Pair Skew | 0.15 $T_{bit}$ |
| Inter-Pair Skew | 0.20 $T_{Pixel}$ |

Where $T_{bit}$ is defined as the reciprocal of Data Transfer Rate and $T_{Pixel}$ is defined as the reciprocal of Clock Rate. Therefore, $T_{Pixel}$ is 10 times $T_{bit}$. In other words, the intra-pair length matching is much more stringent than the inter-pair length matching.

It is recommended that length matching of both signals of a differential pair be within 5 mils. Length matching should occur on a segment by segment basis. Segments might include the path between vias, resistor pads, capacitor pads, a pin, an edge-finger pad, or any combinations of them, etc. Length matching from one pair to any other should be within 100 mils.

Note that lengths should only be counted to the pins or pad edge. Additional etch within the edge-finger pad, for instance, is electrically considered part of the pad itself.

### 2.9.4 ESD Protection for HDMI Interface

**In order to minimize the hazard of ESD, a set of protection diodes are highly recommended for each HDMI Outputs (data and clock).**

International standard EN 55024:1998 establishes 4kV as the common immunity requirement for contact discharges in electronic systems. 8kV is also established as the common immunity requirement for air discharges in electronic systems. International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 establishes the immunity testing and measurement techniques.

System level ESD testing to International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 has confirmed that the proper implementation of Chrontel's recommended diode protection circuitry, using SEMTECH Rclamp0524P diode array devices, will protect the CH7117 device from HDMI panel discharges of greater than 8kV (contact) and 16kV (air). The RClampTM0524P have a typical capacitance of only 0.30pF between I/O pins. This low capacitance won't bring too much bad effect on HDMI eye diagram test.

**Figure 14** shows the connection of HDMI connectors, including the recommended design of SEMTECH Rclamp0524P diode array devices. HDMI connector is used to connect the CH7117 HDMI outputs to the display panels.

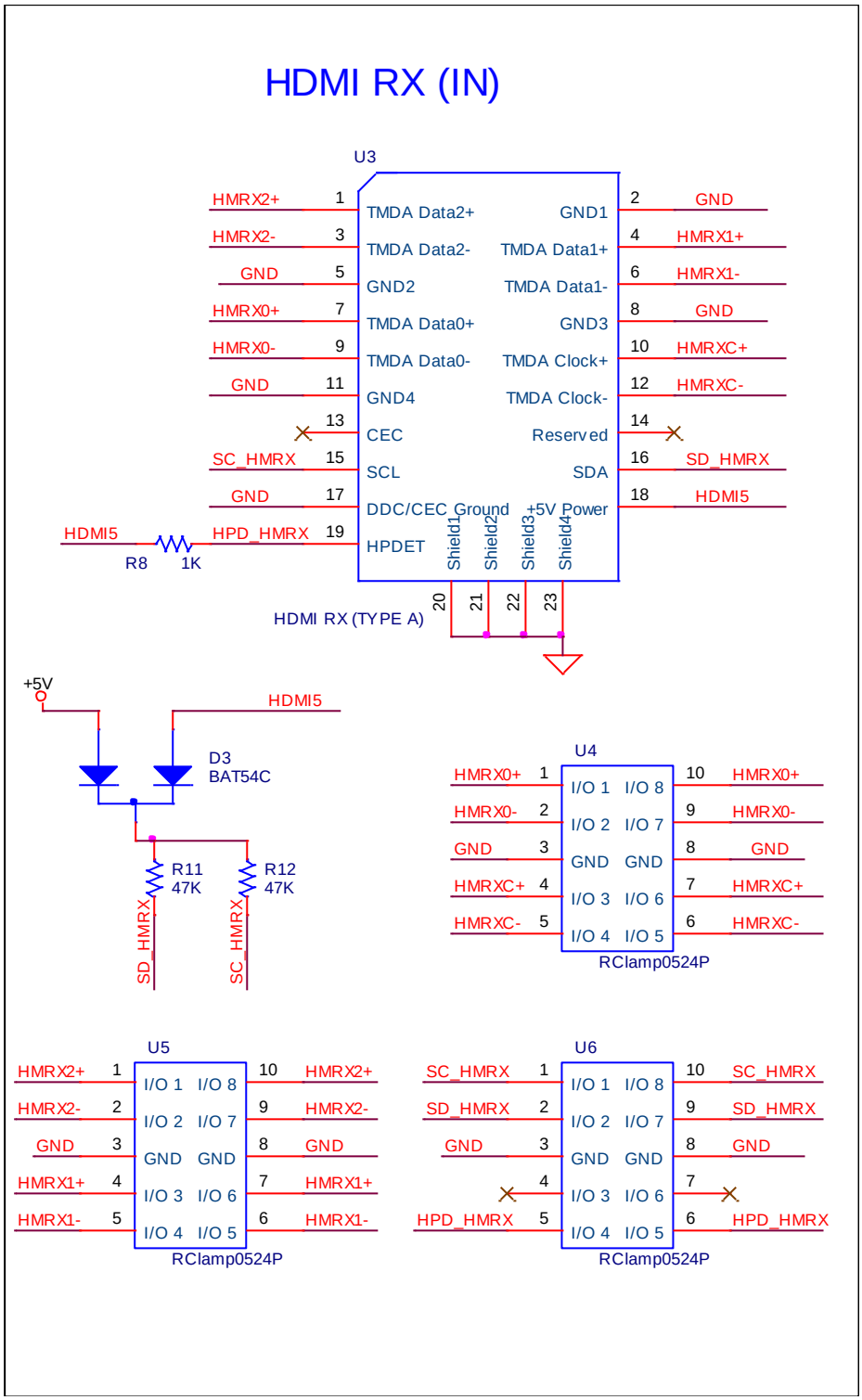


**Figure 14: The connection of the HDMI outputs with ESD protection**

### 2.9.5 Other HDMI signal

**• HPD_HMRX (HDMI Hot Plug)**

This output pin connects to the +5V power through a 1KΩ resistor. Refer to **Figure 14** for the design example.

**•DDC_SD_HMRX and DDC_SC_HMRX**

DDC_SD_HMRX and DDC_SC_HMRX are used to interface with the DDC of HDMI source. The DDC is used by CH7117 to tell source the capabilities and characteristics of the CH7117 by transfer the E-EDID data. This DDC pair needs to be pulled up to 5V through 47K resistors and diodes as shown in **Figure 14**. The diode is used to avoid back drive from DDC signal.

**Note:** Because HDMI source have internal 5V pull-up resistors on DDC trace. In order to avoid back drive, the power for DDC circuit of CH7117 should be independent 5V power supply. Using a diode with low forward voltage is another option. It is better that the forward voltage of the diode does not exceed 0.3V to avoid the voltage on pull-up resistors drops too low.

## 2.10 DAC Output Pins

CH7117 has three separate 9-bit video DACs. Corresponding to three DACs, CH7117 has three DAC output pin, DAC0, DAC1 and DAC2. An internal analog switch can switch DAC0 signal to DAC0 pin or CVBS pin.

**•CVBS Output**

The CVBS signal is analog video signal which comes from DAC0. A 75 Ω resistor should be placed between DAC0 pin and the ground as shown in **Figure 15**. A low pass filter is used to improve the quality of CVBS signal.

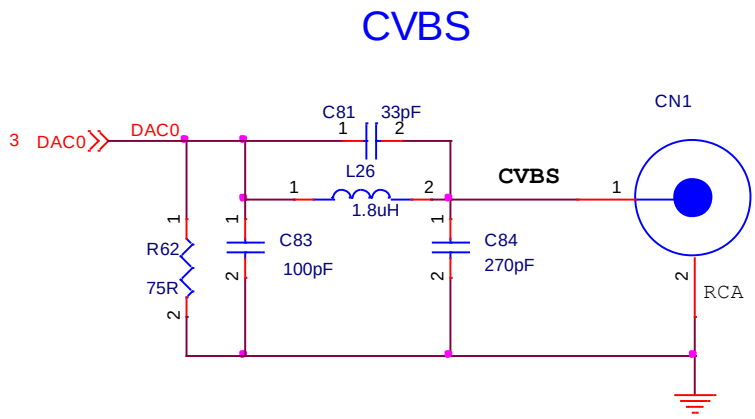


**Figure 15: The CH7117 CVBS outputs**

**•S-Video Output**

The S-Video signals include Y and C components output from DAC1 and DAC2 separately. A 75 Ω resistor should be placed between DAC pin and the ground as shown in **Figure 16**. A low pass filter is used to improve the quality of S-video signal.

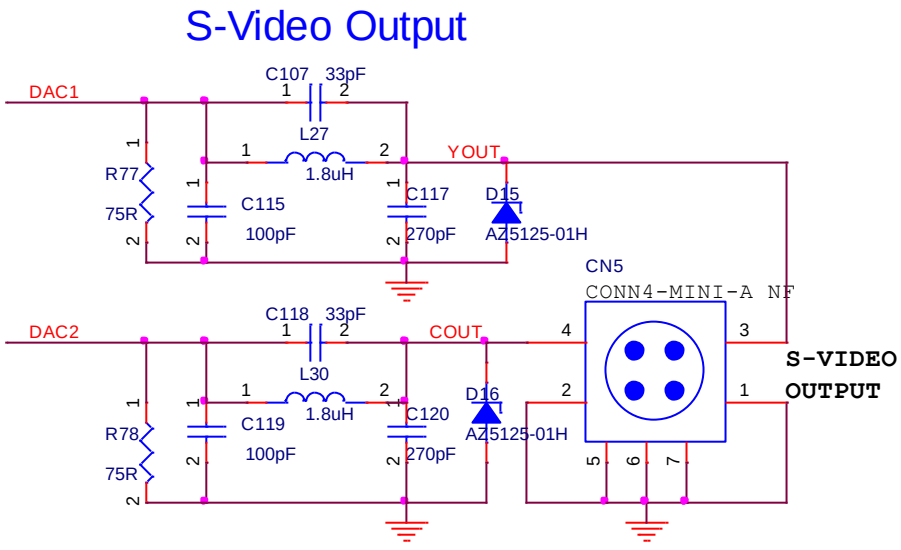


**Figure 16: S-Video**

**•Y/Pb/Pr Output**

The S-Video signals include Y, Pb and Pr components come from DAC0, DAC1 and DAC2 separately. A 75 Ω resistor should be placed between DAC pin and the ground as shown in **Figure 17**. A low pass filter is used to improve the quality of S-video signal.

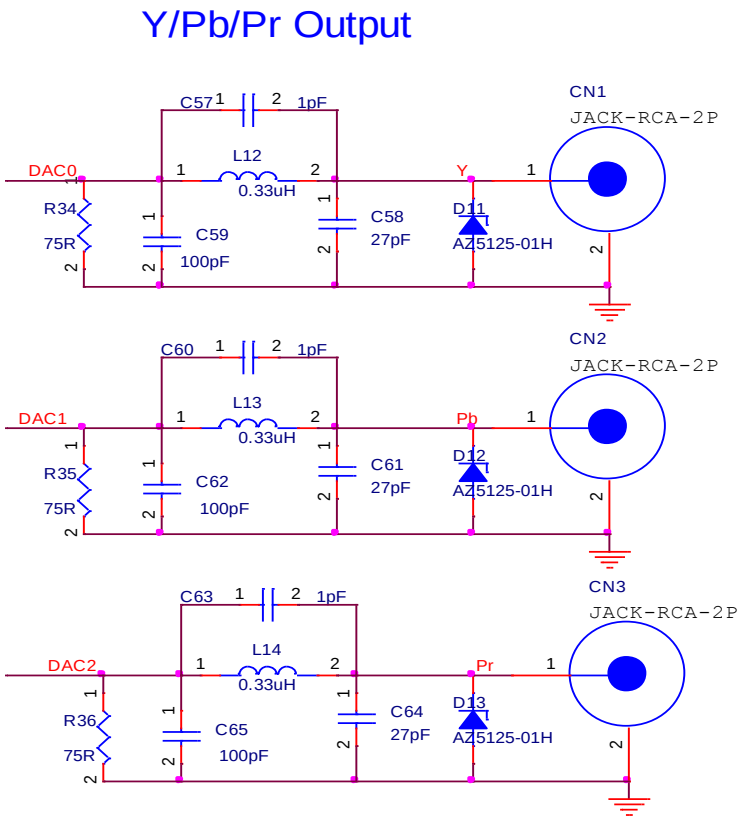


**Figure 17: Y/Pb/Pr Output**

**• VGA_DDC_SC and VGA_DDC_SD**

VGA_SCL and VGA_SDA are used to interface with the DDC of VGA monitor. This DDC pair needs to be pulled up to 5V through 1.8K resistors as shown in **Figure 18**. A low instantaneous forward voltage diode is used to avoid back drive current from VGA monitor.

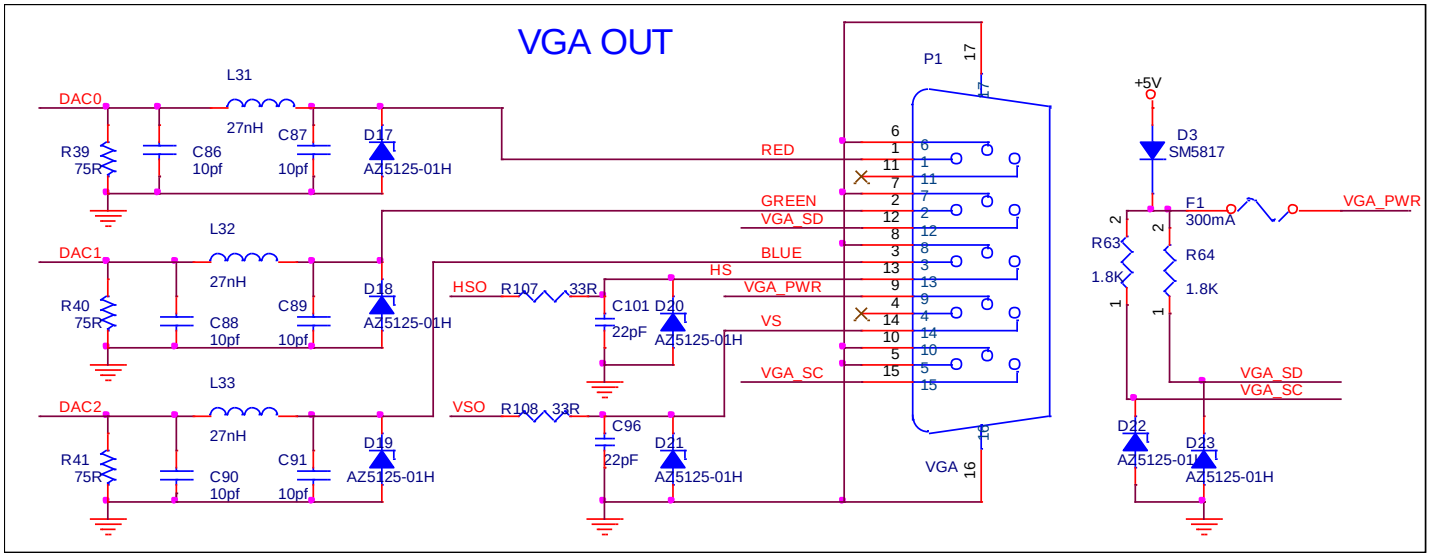


**Figure 18: VGA Output**

## 2.11 Thermal Exposed Pad Package

The CH7117 is available in 88-pin QFN package with thermal exposed pad package. The advantage of the thermal exposed pad package is that the heat can be dissipated through the ground layer of the PCB more efficiently. When properly implemented, the exposed pad package provides a means of reducing the thermal resistance of the CH7117.

Careful attention to the design of the PCB layout is required for good thermal performance. For maximum heat dissipation, the exposed pad of the package should be soldered to the PCB as shown in **Figure 19**.

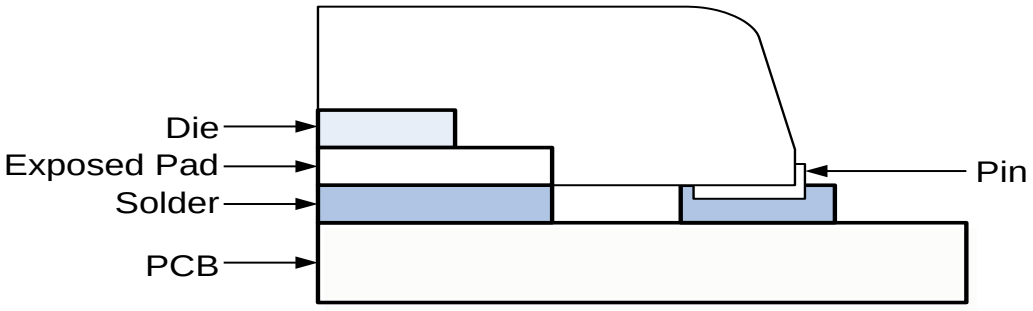


**Figure 19: Cross-section of exposed pad package**

Thermal pad dimension is from 6.6mm to 6.9mm (min to max), 6.6mm x 6.6mm is the minimum size recommended for the thermal pad, and 6.9mm x 6.9mm is the maximum size. As shown in **Figure 20**, the thermal land pattern should have a 5x5 grid array of 1.0 mm pitch thermal vias connected to the ground layer of the PCB. These vias should be 0.3mm in diameter with 1 oz copper via barrel plating.

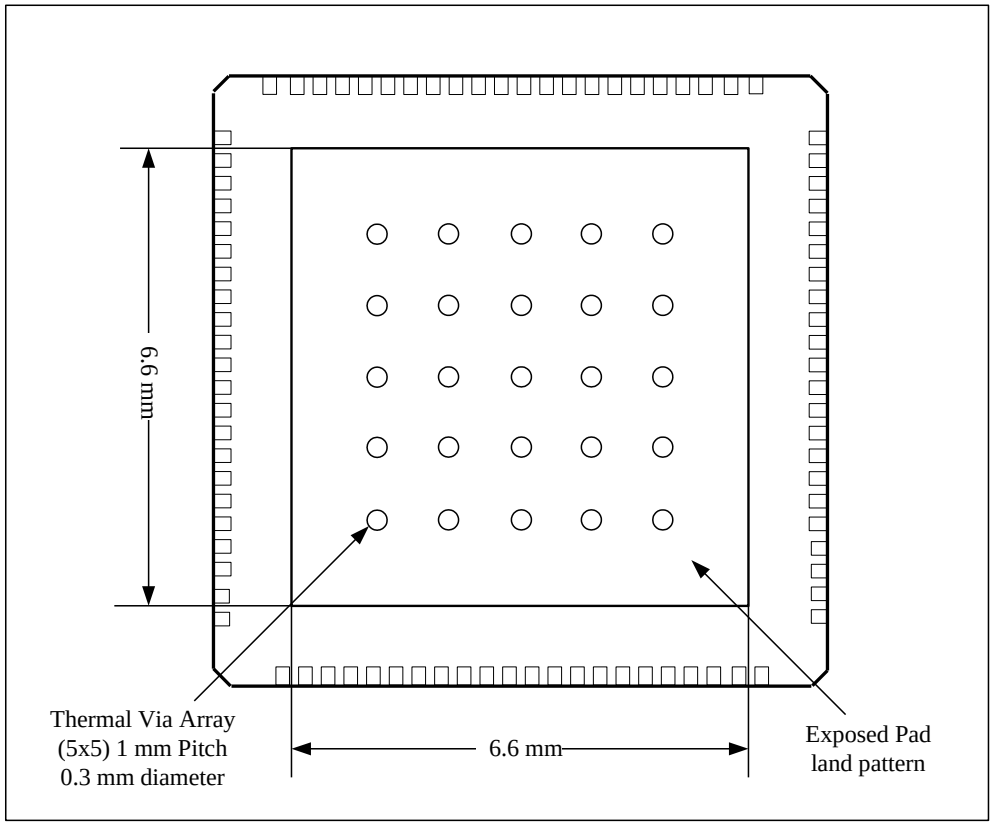


**Figure 20: Thermal Land Pattern**

When applying solder paste to the thermal land pattern, the recommended stencil thickness is from 5 to 8 mils. Thermal resistance was calculated using the thermal simulation program called ANSYS.

For the assembly process, it is important to limit the amount of solder paste that is put under the thermal pad. If too much paste is put on the PCB, the package may float during assembly. Compared with the solder mask of thermal pad, the paste mask should be shrank to70%~80%.

## 2.12 Others about PCB layout

To ensure the CH7117 can work properly, the PCB layers should not be less than 4 layers.

The DC/DC switching regulator and power inductor should be placed 270mil away from the ISET pin of CH7117. At most one via can be used on trace.

# 3.0 REVISION HISTORY

**Table 10: Revisions**

| Rev. # | Date | Section | Description |
|---|---|---|---|
| 0.9 | 2020/06/30 | All | |
| 1.0 | 2021/11/04 | Section 2.0<br>Section 2.2<br>Section 2.12 | 2.0 Add 100pf on ISET pin<br>2.2 Update Reset and CH7117 State<br>2.12 Add PCB layout description |

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**Chrontel**

**www.chrontel.com**

**E-mail: sales@chrontel.com**

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